

GX5960 SERIES

PRELIMINARY DATASHEET

6U PXI HIGH PERFORMANCE DYNAMIC DIGITAL I/O SUBSYSTEM

- Cycle based, 50 MHz dynamic digital subsystem with high performance timing generator
- High voltage pin electronics with per channel programmability
- Per channel parametric measurement unit (PMU)
- Analog bus access for each I/O channel
- Dual level drive / sense, and programmable load on a per channel basis
- 256 timing sets with 4 phases and 4 windows
- 0 - 64 us phase and window programming range
- Supports up to 528 bi-directional I/O channels
- 256K of vector memory
- Comprehensive software tool set supports CASS legacy programs and importing of IEEE – 1445 compliant vector files



DESCRIPTION

The GX5960 digital subsystem represents the highest level of performance available for PXI-based digital instrumentation. Based on the proven architecture of the GX5055 and the EADS T964, the GX5960 offers high performance pin electronics and a timing generator / sequencer in a compact, 6U PXI form factor. The GX5960 series consists of one GX5961 Clock generator board with 16 driver / sensor channels and the GX5964 driver / sensor board which supports 32 bi-directional I/O channels. Up to 528 digital I/O channels can be supported by the GX5290 digital subsystem. Each digital channel features a wide drive / sense voltage range of -15 V to +25V (maximum swing of 26 volts) which can be individually programmed for a drive hi, drive lo, sense hi, sense lo, and a load value (with commutation voltage level) – offering the user complete flexibility when creating test programs and fixtures for multiple UUTs. In addition, each channel offers a parametric measurement unit (PMU) for DC measurements.

FEATURES

The GX5960 offers real-time digital stimulus, record, or expect data modes on all I/O channels. Pattern memory depth is 256K words. Each channel can be configured as an input or output on a per cycle basis. Six drive data formats are supported: NR, R1, R0, RZ, RC, and Complement Surround – providing flexibility to create a variety of bus cycles and waveforms to test board and box level products.

The GX5961 provides timing, input / output synchronization signals, and sequencing as well as 16 I/O channels. Additional channels can be added to the system by installing one or more, GX5964 boards which are interconnected via the PXI local and trigger busses. The

GX5961 offers a flexible clock system which allows the module to operate as a timing master to the UUT or be slaved to the UUT's time base or some other external clock.

All pin electronic resources are independent on a per channel basis – offering the user complete flexibility when programming drive / sense levels, source / sink currents, slew rate, skew, or PMU functions. The PMU can operate in the force voltage / measure current or force current / measure voltage mode and is useful for measuring a UUT's DC characteristics. In addition, each I/O channel includes an analog bus relay, which allows each channel to support hybrid channel (digital or analog) measurement capabilities. For analog stimulus / response measurements, the analog bus can be connected to external resources via a dedicated analog bus connector located on the front panel of the module.

Data Sequencer

The GX5961's sequencer supports sequences up to 4096 steps and has 16 loop counters that may be nested. The sequencer supports a variety of sequencing functions including jumps, subroutines, looping, and test inputs. All of the sequencer commands may be programmed using a Graphical Vector Editor, Windows® API commands, or via a script language. The sequencer allows the user to generate test vectors indefinitely at maximum test rates. Internal and external trigger and pause commands are available in several modes.

Timing Generator

The GX5961's timing generator supports 256 timing sets which can consist of up to 4 drive phases and 4 sense windows for 4K of

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sequence steps. Alternative timing set configurations include 1K of timing sets with 4 phases and 4 sense windows or 4K of timing sets with 1 phase and 1 window. The T0 cycle or sequencer period range is programmable from 20 ns to 64 us with the phase and window values programmable from 0 ns to 64 us. This flexibility offers the user the ability to address a wide range of applications including the emulation of complex bus cycles and proprietary digital interfaces.

Compatibility

The GX5960 subsystem can operate in any 6U PXI chassis that supports an air flow rate of 20 cfm/slot. Power for the pin electronics requires the use of external power supplies or the GX5960 can be used with a Geotest GX7005A / GX7015A PXI chassis which is designed specifically for high performance / high power digital applications and includes the necessary pin electronics power supplies.

SOFTWARE

The GX5960 is supplied with DIOEasy, a software package that includes vector editing, a virtual instrument panel, and 32-bit DLL driver libraries and documentation. The virtual panel can be used to interactively program and control the instrument from a window that displays the instrument's current settings and status. In addition, interface files are provided to support access to programming tools and languages such as ATEasy, Microsoft® and Borland® C/C++, Microsoft Visual Basic®, Borland Delphi, and Pascal.

Other optional software packages are available to support the importing of CASS digital TPS' or IEEE-1445 .tap files.

APPLICATIONS

- Automatic Test Equipment (ATE)
- High-speed functional digital test
- Vector capture
- Hybrid and digital device test
- Memory testing
- LRU and SRU test

SPECIFICATIONS

TIMING	
INTERNAL TEST CLOCK OR SYSTEM CLOCK (TO_CLK)	15.625 KHz to 50 MHz (using the 500 MHz master clock)
TEST CLOCK TIMEBASE	Ext Reference Clock: 1 MHz to 80 MHz Internal reference clock: 20 MHz

TO_CLK TIMING RESOLUTION	2 ns (using the 500 MHz master clock)
MASTER CLOCK (PHASE AND WINDOW TIMING SOURCE)	500 MHz (internal oscillator), +/- 50 ppm 40 KHz to 500 MHz (PLL), +/- 50 ppm
MASTER CLOCK REFERENCE	Internal: 20 MHz PXI CLCK10 Front panel: 5 MHz to 80 MHz
TIMING SET OPTIONS	<ul style="list-style-type: none"> •256 Timing Sets with 4 Phases, 4 Windows, and 4K sequence steps •1 K Timing Sets with 4 Phases, 4 Windows, and 1 K sequence steps (one timing set for each sequence step) •4K Timing Sets with 1 Phase, 1 Window, and 4K sequence steps (one timing set for each sequence step)
PHASE PROGRAMMING RANGE (ASSERT / RETURN)	0 ns to 64 us (using the 500 MHz master clock)
WINDOW PROGRAMMING RANGE (OPEN / CLOSE)	0 ns to 64 us (using the 500 MHz master clock)
PHASE & WINDOW TIMING RESOLUTION	1 ns, using the 500 MHz master clock
MINIMUM PHASE / WINDOW PULSE WIDTH; ASSERT / RETURN OR OPEN / CLOSE	8 ns, using the 500 MHz master clock
PHASE / WINDOW REFERENCE	Phases: System or Pattern Clock (selectable per Seq Step) Windows: Pattern clock only
PHASE / WINDOW DEAD TIME	10 ns at end of the Pattern period (using 500 MHz master clock)
CLOCKS PER PATTERN	1 to 256 (selectable per Seq Step)
PAUSE / PATTERN CLUTCH	Phases and Windows are frozen when Pause is asserted Pause on external event Pause based on phase edge Resume after programmed delay Resume on an external signal or CPU resume
HALT / SYSTEM CLUTCH	Halt based on an external signal Halt on error Halt on a Sync pulse (used as a breakpoint)
PAUSE / PATTERN AND HALT / SYSTEM CLUTCH SOURCES	PXI trigger lines Aux I/O 1-12 Ch. 1-32 (with mask/expect), (GX5964) Ch. 1-16 (with mask / expect), (GX5961) Phase 1-4 (for Pause)
DRIVE / SENSE MODES & CHANNEL I/O SPECIFICATIONS (ALL SPECIFICATIONS BASED ON PIN ELECTRONIC VOLTAGE RAILS (VCC AND VEE) OF +18 AND -14 V)	
NUMBER OF I/O CHANNELS	16 per card (GX5961) 32 per card (GX5964)
TEST MODES	Dynamic or Static
DATA OUTPUT FORMATS (PER CHANNEL)	Drive Hi, Drive Lo, Hi-Z Formatted Data: No return, Return to 1, Return to 0, Return to Hi-Z, Return to complement, Surround by complement; selectable on a per channel basis
DRIVE DATA TIMING (PER CHANNEL)	Data assert / de-assert based on Phases 1-4

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CAPTURE MODES (PER CHANNEL)	Mask Opening edge of Window Closing edge of Window Window – data is valid for entire window duration
DRIVE / EXPECT MODE	Output: Drive Hi, Drive Lo, Hi-Z Expect: 1, 0, OK, between states, or mask Keep last Toggle last Accumulate CRC-16
RECORDING MODES (PER SEQUENCE STEP)	Record errors for programmable inputs that have Good 1 & Good 0 Record errors for inputs that have only a Good 1 Record raw data based on NOT a Good 0 Record raw data based on a Good 1
ERROR ADDRESS RECORD	Record address for memory errors 1K deep error memory
NUMBER OF DRIVE AND SENSE VOLTAGE REFERENCES	GX5961: •16 Drive Hi / Drive Lo •16 Sense Hi / Sense Lo GX5964: •32 Drive Hi / Drive Lo •32 Sense Hi / Sense Lo
DRIVE VOLTAGE LEVEL	Drive Hi: -9 to +15V Drive Lo: -10 to + 11V
DRIVE VOLTAGE LEVEL RANGE	Min: 0.5 V p-p Max: 26 V p-p
DRIVE VOLTAGE ACCURACY	+/- 25 mv, < 26 V p-p drive voltage
DRIVE VOLTAGE RESOLUTION	16 bits
OUTPUT IMPEDANCE	50 ohms, typical
DRIVE CURRENT	200 mA per channel 1.6 A per board, max (GX5964) .8 A per board, max (GX5961)
SHORT CIRCUIT PROTECTION	Programmable current level with automatic disable, per channel basis
SLEW RATE	.1 to 1 V/ns, adjustable, programmable on a per channel basis
CHANNEL SKEW	160 ps, typical 320 ps max., after calibration, for all channels (Drive and sense)
CHANNEL DE-SKEW	Range: +/- 5 ns Resolution: 312.5 ps - Programmable on a per channel basis. - Separate deskew control for drive and sense.
SENSE VOLTAGE RANGE	Sense Hi: -10 to +11 V Sense Lo: -10 to +11 V
SENSE VOLTAGE THRESHOLD ACCURACY	+/- 25 mv, < 26 V p-p sense voltage
SENSE VOLTAGE RESOLUTION	16 bits
INPUT LEAKAGE CURRENT	50 nA, max

PULL-UP / PULL-DOWN CURRENT SOURCE/ SINK	+/- 24 ma, programmable on a per channel basis V commutate: -10 to +11 V., programmable on a per channel basis
PULL-UP / PULL-DOWN CURRENT SOURCE / SINK ACCURACY	+/- 250 uA
PULL-UP / PULL-DOWN CURRENT SOURCE / SINK RESOLUTION	16 bits
VOLTAGE COMMUTATION ACCURACY	+/- 25mv, < 25 V range
VOLTAGE COMMUTATION RESOLUTION	16 bits
RESISTIVE LOAD	Range: Hi-Z, 250 ohm, 1 K ohm, programmable on a per channel basis
MEMORY	256K words
SEQUENCER	
COMMANDS	Jump, Conditional Jump, Loop, Call Subroutine, Return, Pause, Halt
LOOP COUNTERS	16, can be nested Only one can end on a sequence step Loop count range: 1 – 64K or continuous
TEST INPUTS	External: PXI triggers, Aux I/O Internal: Data sense, Edge or level
SEQUENCER MEMORY	1024 or 4096 Steps
PATTERN CLOCK (PAT_CLK)	1-255, T ₀ _CLK periods
PHASE TRIGGER	T ₀ _CLK or PAT_CLK
WINDOW TRIGGER	PAT_CLK
PATTERNS PER SEQUENCE STEP	1 to 256K
WAVEFORM ENABLE	1 to 4
WAVEFORM NUMBER	0 to 255
SEQUENCE LOOP	1 to 1M, continuous
CURRENT STEP LOOP	1-65535, continuous
MULTI STEP LOOP	1-65535, nested 16 deep
JUMP	Conditional / Unconditional
JUMP CONDITIONS	Error True, Sequence Timeout True, Signal Level (High / Low), Signal Edge (Rising / Falling)
JUMP SIGNAL SELECTIONS	Aux1 – Aux12, PXI Triggers, CHT1 (mask and expect for all 32 channels)
SEQUENCE FLAGS	2
GX5961 TIMING GENERATOR BOARD EXTERNAL TIMING, CONTROL AND STATUS SIGNALS	
SYNC OUTPUTS	2, Start of Sequence; Start of Sequence Step
GENERAL PURPOSE AUX I/O	12 64 output selections 7 input selections
INPUT AUX I/O SELECTIONS	Synthesizer reference clock, System clock, Break (System Clutch), Halt (Pattern Clutch), Sequence Jump signals
OUTPUT AUX I/O SELECTIONS	Phase, Window, Waveform, Syncs, Seqflag, Seq Active, Seq Idle, T ₀ _Clk, Pat_Clk, misc test signals.
PROBE	Ground, Probe Button, Probe LED, Monitor

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ORDERING INFORMATION

PARAMETRIC MEASUREMENT UNIT (PMU)	
NUMBER OF PARAMETRIC MEASUREMENT UNITS	32, one per channel (GX5964) 16, one per channel (GX5961)
MODES	Force voltage, measure current Force current, measure voltage
FORCE VOLTAGE RANGE	- 10 volts to + 15 volts
FORCE VOLTAGE ACCURACY	+/- 25 mV, 25 volt range
FORCE VOLTAGE & CURRENT RESOLUTION	16 bits
FORCE CURRENT RANGE	+/- 30 mA FS +/- 200 mA FS
FORCE CURRENT ACCURACY	+/- 100 uA, 30 mA range +/- 8 mA, 200 mA range
MEASURE VOLTAGE RANGE	-10 to +15 volts
MEASURE VOLTAGE & CURRENT RESOLUTION	16 bits
MEASURE VOLTAGE ACCURACY	+/- 15 mV, -9 to +13 volt range
MEASURE CURRENT RANGE	+/- 30 ma FS +/- 200 ma FS
MEASURE CURRENT ACCURACY	+/- 100 uA, (30 mA range) +/- 6 mA (200 mA range)
ANALOG MEASUREMENT BUS	
NUMBER OF ANALOG I/O CHANNELS	16 per card (GX5961) 32 per card (GX5964)
CONTROL	Independent connect / disconnect to each I/O channel
ENVIRONMENTAL	
OPERATING TEMPERATURE	0 to 50° C
STORAGE TEMPERATURE	-20° C to +70° C
VIBRATION	5 g at 500 Hz
SHOCK	10 g for 6 ms ½ sine
PHYSICAL DIMENSIONS	
SIZE	6U PXI , single slot
WEIGHT	1.2 lbs (520 g)
CONNECTIONS (GX5961 & GX5964)	
ANALOG BUS (FOR CONNECTIONS TO ANALOG INSTRUMENTATION)	68 position SCSI III Type
I/O, EXTERNAL CONTROL, TIMING	68 position SCSI III Type
EXTERNAL VCC / VEE	15 position D-sub, male +18 volts @ 6 A (GX5964) @ 3 A (GX5961) -14 volts @ 6 A (GX5964) @ 3 A (GX5961)

GX5961	50 MHz, Timing Generator PXI card. 16 channels with 256K of memory per channel. Includes DIOEasy and Data I/O cable. One card required per domain.
GX5964	50 MHz, high performance dynamic digital I/O PXI card. 32 channels with 256 K of memory per channel. Includes Data I/O cable
ACCESSORIES	
GT8XXX	DtifEasy - Includes LASAR conversion tool, probe and ATEasy Test Executive and Application Development Environment
GT95014	Connector interface, SCSI to 100 Mil Grid, Single Ended I/F Board
GT95021	2' shielded cable (68-pin SCSI)
GT95022	3' Shielded cable (68-pin SCSI)
GT95028	10' Shielded cable (68-pin SCSI)
GT95031	6' Shielded cable (68-pin SCSI)

Note: Specifications are subject to change without notice.