

GX5152 SERIES

DIGITAL STIMULUS RESPONSE INSTRUMENT

- 100 MHz timing module with 32 digital input or output channels (GX5152)
- 50/100 MHz with 32 channels digital input or output (GX5153)
- 1 MB to 32 MB of on-board memory
- Up to 15 slave cards for a total of 512 pins
- Fully compatible with Summation SigmaSeries DSR10 and DSR11
- Control and synchronize PXI Trigger Bus with 10 ns resolution
- 6U PXI board



DESCRIPTION

The GX5152 Series is a family of 6U PXI instruments that provide extensive high speed digital I/O capability. The GX5152 Digital Stimulus Response (DSR) instrument is the master, providing the timing set and 32 channels of digital input or output. The GX5153 slave provides 32 channels of digital input or output based on the timing set provided by the GX5152. Additional GX5153s may be added to expand the dynamic digital I/O channels up to 512 channels.

FEATURES

The GX5152 controls all timing using a dedicated local bus and the PXI Trigger Bus. Similar to the Summation SigmaSeries DSR10, the GX5152 provides strobes to signal the host and any slave GX5153 PXI instruments to generate or capture data. These strobes are fast, repetitive timing signals (for example, the address and data bus strobes in a bus emulation application). The GX5152 features 10 ns edge placement resolution.

An internal finite state machine produces a sequence of output states that make up the timing set or "Major Cycle". Major Cycle refers to a bus cycle or clock cycle depending on the device or unit under test interface. A timing set can contain up to 256 unique output states. Each state defines the logic level of each high speed strobe output. The timing module dedicates two more state outputs to generate or record vectors into the main pattern memory.

The Trigger signal initiates the execution of vector capturing (or vector stimuli). The multiple software and hardware trigger sources provide flexibility in synchronizing the GX5152 with real world events. External trigger source and qualifiers work to start or stop overall operation. Two flags separately or combined (AND / OR) pause the Major Cycle until an internal or external signal meets the test condition.

The GX5152 offers a variety of I/O modules. The I/O modules are daughter boards that mount directly on the GX5152 board. Available I/O modules include TTL, PECL, ECL, Programmable Levels, Frequency Doubler, and LVDS.

The Timing Module provides clocks, strobes, and additional timing signals to control the timing of the GX5152. The Timing Module Level Adapter (TMLA) is a daughter board that mounts on the Timing Module to change the levels according to the selected I/O module (TTL, PECL, ECL, LVDS, or programmable levels). The default TMLA is TTL.

Additionally, the GX5152 accommodates between two and five memory SIMMs. One SIMM is used by the sequencer, and the other four by the I/O pins. Each SIMM provides 256 Kb, 1Mb, or 2 Mb per pin, for a maximum of 8 Mb. The GX5152 architecture enables the user to stack the memory to reconfigure the board as a 16-pin I/O with 16 Mb depth or as an 8-pin I/O providing a maximum of 32 Mb behind each pin.

SOFTWARE

The GX5152 Series is supplied with a virtual instrument panel, which includes the 32-bit DLL driver libraries and documentation. The virtual panel can be used to interactively adjust and control the instrument from a window that displays the current instrument set-tings and measurements.

In addition, various interface files provide access to the library for programming tools and languages such as ATEasy, Microsoft® and Borland® C/C++, Microsoft Visual Basic®, Borland Delphi, LabVIEW, and more.

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APPLICATIONS

- Board Automatic Test Equipment (ATE)
- Bus Emulation
- A/D and D/A testing
- ASIC, FPGA, and CPLD testing
- Precision pattern generation
- Precision pattern capture
- Non-standard frame capturing
- Gang testing of boundary scan devices

SPECIFICATIONS

TIMING MODULE	MIN	MAX
INTERNAL TEST CLOCK		
FREQ. RANGE	5 Hz	100 MHz
RESOLUTION	The greater of 1Hz or 0.01%	
INTERNAL B CLOCK		
FREQUENCY RANGE	1 MHz	100 MHz
RESOLUTION	The greater of 1Hz or 0.2%	
EXTERNAL CLOCK		
DIRECT	0 Hz	50 MHz
REF FOR PROG.	1 MHz	60 MHz
PULSE WIDTH	10 ns	
INPUT LEVEL		
LOW	-0.1 V	0.8 V
HIGH	2.0 V	5.1 V
INPUT/OUTPUT		
CHANNELS PER MODULE	3 programmable configurations: 8-bit, 16-bit, and 32-bit I/O	
I/O MEMORY	256 Kb Max.	
PHYSICAL		
TEMPERATURE OPERATING STORAGE	0° C to 50° C -20° C to 70° C	
SUPPLY CURRENT	MIN	MAX
@ 5 V _{DC}	200 mA	500 mA
@ 12 V _{DC}	50 mA	100 mA
WEIGHT	100 g	
SIZE	6U PXI	
PXI SLOT TYPE	Double Slot (GX5152); Single Slot (GX5153)	
PC INTERFACE	Windows 95/NT Plug and Play or Legacy (Selectable)	

ORDERING INFORMATION

GX5152	6U PXI High Speed Digital Stimulus Response Master
GX5153	6U PXI High Speed Digital Stimulus Response Slave
GX5910	TTL I/O module
GX5920	Frequency Doubler I/O module
GX5930	Programmable levels I/O Module
GX5940	PECL I/O Module
GX5960	LVDS I/O Module
GX5970	Differential TTL I/O Module
GT5006	256 Kb Memory SIMM for GX5152
GT95014	Connector interface for GX5xxx/GX5732, SCSI to 100 Mil Grid, Single ended
GT95015	Connector interface for GX515x, SCSI to 100 Mil Grid, Differential
GT95020	Connector I/F for GX515x, SCSI to 100 Mil Grid, Single ended (both 64 & 14-pin)
GT95021	2' shielded cable for GX5xxx (68-pin)
GT95022	3' shielded cable for GX5xxx (68-pin)
GT95028	10' shielded cable for GX5xxx (68-pin)
GT95028	10' shielded cable for GX5xxx (68-pin)

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PIN ASSIGNMENT

68-PIN UUT I/O DATA CONNECTOR, J2			
IO0+	1	35	IO0-
IO1+	2	36	IO1-
IO2+	3	37	IO2-
IO3+	4	38	IO3-
IO4+	5	39	IO4-
IO5+	6	40	IO5-
IO6+	7	41	IO6-
IO7+	8	42	IO7-
IO8+	9	43	IO8-
IO9+	10	44	IO9-
IO10+	11	45	IO10-
IO11+	12	46	IO11-
IO12+	13	47	IO12-
IO13+	14	48	IO13-
IO14+	15	49	IO14-
IO15+	16	50	IO15-
IO16+	17	51	IO16-
IO17+	18	52	IO17-
IO18+	19	53	IO18-
IO19+	20	54	IO19-
IO20+	21	55	IO20-
IO21+	22	56	IO21-
IO22+	23	57	IO22-
IO23+	24	58	IO23-
IO24+	25	59	IO24-
IO25+	26	60	IO25-
IO26+	27	61	IO26-
IO27+	28	62	IO27-
IO28+	29	63	IO28-
IO29+	30	64	IO29-
IO30+	31	65	IO30-
IO31+	32	66	IO31-
VTHI	33	67	VTHI1
VTLO	34	68	VTLO1

Note: For non-differential I/O modules, all IOx- (negated) lines are grounded.

68-PIN UUT CONTROL CONNECTOR, J1			
GND	1	35	GND
N/C	2	36	N/C
N/C	3	37	N/C
N/C	4	38	N/C
N/C	5	39	N/C
GND	6	40	GND
N/C	7	41	N/C
N/C	8	42	N/C
N/C	9	43	N/C
N/C	10	44	N/C
GND	11	45	GND
N/C	12	46	N/C
N/C	13	47	N/C
SCLK	14	48	GND
SSYNCCC	15	49	GND
SDOUT	16	50	GND
SDIN	17	51	GND
GND	18	52	GND
OEN0	19	53	GND
OEN1	20	54	GND
OEN2	21	55	GND
OEN3	22	56	GND
GND	23	57	GND
XOE0	24	58	GND
XOE1	25	59	GND
XOE2	26	60	GND
XOE3	27	61	GND
GND	28	62	GND
JA	29	63	GND
N/C	30	64	GND
5V	31	65	GND
5V	32	66	GND
VTHI	33	67	VTHI
VTLO	34	68	VTLO

Notes: JA-Jump to a pre-defined address A Input. A low on this line will cause a jump to that address.

OEN0-OEN3-IOM generated Output Enables. A low on these lines specifies the I/O group currently enabled.

SCLK, SDOUT, SDIN, SSYNCCC-should not be connected at any time.

XOE0-XOE3-External Output Enable input controls for each I/O group. A low on these lines will force the specific group to disable its output drivers.

68-PIN (VHD) TO UUT TIMING CONNECTOR, J1			
Q0+	1	35	Q0-
Q1+	2	36	Q1-
F0+	3	37	F0-
F1+	4	38	F1-
STOP+	5	39	STOP-
START+	6	40	START-
TRIG+	7	41	TRIG-
NU	8	42	NU
UStrb0+	9	43	UStrb0-
UStrb1+	10	44	UStrb1-
UStrb2+	11	45	UStrb2-
UStrb3+	12	46	UStrb3-
UStrb4+	13	47	UStrb4-
UStrb5+	14	48	UStrb5-
UStrb6+	15	49	UStrb6-
UStrb7+	16	50	UStrb7-
ARM+	17	51	ARM-
ORUN+	18	52	ORUN-
GND	19	53	GND
BLCK+	20	54	BCLK-
GND	21	55	GND
OCLK+	22	56	OCLK-
GND	23	57	GND
OSTB+	24	58	OSTB-
GND	25	59	GND
XTRIG+	26	60	XTRIG-
XPAUSE+	27	61	XPAUSE-
XCEN+	28	62	XCEN-
XSTBEN+	29	63	XSTBEN-
GND	30	64	GND
XCLK+	31	65	XCLK-
XSTB+	32	66	XSTB-
VTHI	33	67	VTHI
VTLO	34	68	VTLO

Note: OCLK-Clock Output is not valid when using External Clock Enable (XCEN) with External Clock Input (XCLK).

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DIGITAL I/O